Capacitor-Free Leaky Integrator for Biomimic Artificial Neurons

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Indexing terms: artificial neurons, leaky integrator, metal-oxide-semiconductor structures and devices.

A method for implementing capacitor-free leaky integrators for biomimic artificial neurons is presented. The method employs a low-gain non-inverting amplifier with nonlinear feedback resistors implemented from PMOS devices operating in the triode region.

Introduction: The leaky integrator is a key subsystem in pulse-mode artificial neuron implementations [1]. In most implementations reported to date this function has been implemented with the explicit use of integrated capacitors and with fixed time constants. More recently it has been noted that mimicking real biological systems is better accomplished if the integrator time constants are adaptable and if different time constants are realized for rising and falling edges of the circuit's pulse response. One such implementation was reported in [2]. This implementation used a PMOS transistor in the triode region as a nonlinear feedback resistor, a high-gain inverting amplifier, and two capacitors to effect a voltage-dependent active filter transfer function.

Here we present a capacitor-free integrator that obtains voltage-dependent and asymmetric rise and fall times. Integrating action is obtained through the use of nonlinear resistors realized using triode-region-biased PMOS transistors operated near the weak inversion region. This enables us to take advantage of their parasitic capacitance to obtain large time constants from an active filter topology using a low-gain non-inverting amplifier.

Circuit: The circuit implementation is shown in Figure 1. PMOS transistors M1 and M2A-E comprise the feedback resistors. We refer to these devices as "delay resistors" since it is the RC time constants due to these devices which effects the circuit's integration response characteristics. These devices have identical geometry with width-to-length (W/L) ratios of 3 μm / 3 μm.

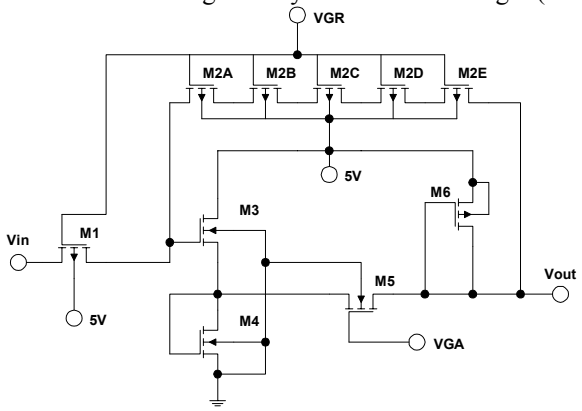

Fig. 1 Leaky integrator circuit.

NMOS transistors M3 – M5 and PMOS transistor M6 comprise a common-gate amplifier designed to have a nominal small signal gain of 2.5 V/V for positive-going input signals at the quiescent bias point (Q-point). M3, M4, and M5 have W/L ratios of 20/5, 50/5, and 50/5 respectively. Q-point drain current for M5 is 68 nA, of which 51 nA is drawn through M2, when V_{GR} is 1.0 volts and V_{GA} is 2.2 volts. Under these conditions the Q-point output voltage V_{OUT} is 2 volts for V_{IN} equals 2.6 volts. PMOS load device M6 has W/L = 4/5. The process parameters assumed are for a 1.5 micron MOSIS™ process.

Pulse response: Dynamic response of this circuit is a function of the delay-resistor bias V_{GR} and the input signal level V_{IN}. Our input Q-point design is 2.6 volts. Figure 2 shows the response of the circuit as a function of V_{GR} to a 0.25 volt input pulse over a range of V_{GR} from 1.0 to 1.4 volts in 0.1 volt increments. The slowest response is obtained for V_{GR} = 1.4 volts and speeds up as V_{GR} is decreased. The input is the square pulse shown at the top of the figure.

This response is qualitatively easy to understand. The delay resistor M2 time constant goes approximately as

$$\tau = \frac{2L^2}{\mu\left[2(V_{SG} - V_T) - V_{SD}\right]} \qquad (1)$$

where V_{SG} is the source-to-gate voltage, V_T is the threshold voltage, V_{SD} is the source-to-drain voltage and μ is the carrier mobility. In response to a positive-going input V_{SG} increases whereas the use of multiple transistors in M2 keeps V_{SD} from matching this increase despite the gain of the amplifier. This accounts for the relatively rapid rising edge of

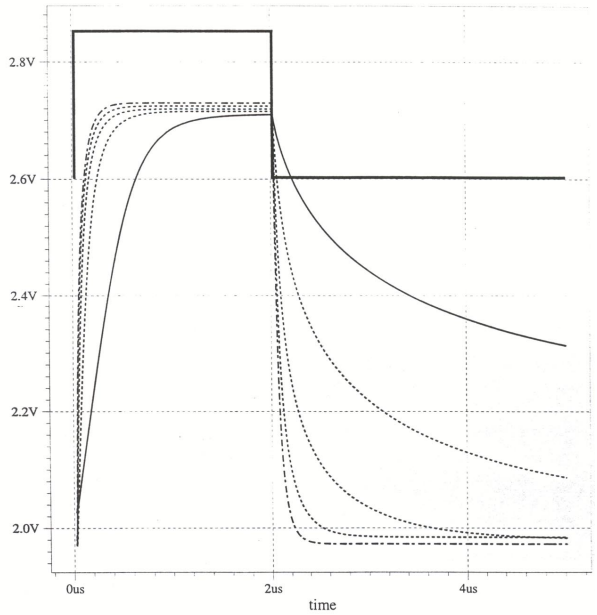

Fig. 2 Pulse response as a function of delay-resistor gate bias. The input signal is the top trace. The solid trace is the output at V_{GR} = 1.4 volts. V_{GR} is reduced in 0.1 volt steps for the other output voltage traces.

the circuit response. On the falling edge, however, we have decreasing V_{SG} and consequently an increasing τ on the falling edge. This property of MOSFET devices used as resistors has been previously discussed [3]. At the higher settings of V_{GR} the M2 device leaves the strong inversion region and very low M2 conductance at the Q-point results.

The circuit response is a function of input signal level. Figure 3 illustrates the response of the circuit to input pulses of 0.1 through 0.35 volts in 50 mV steps for V_{GR} = 1.3 volts. Slower responses are obtained for the lower-level input signals. The mechanism here is the same as that of (1). Risetime response time decreases up to an ac input of 0.25 volts. The anomalous risetime response for 0.30 volts is due to a nonlinearity in the transfer characteristic of the amplifier and is caused by the V_{GS} of M5 leaving the strong inversion region. The apparent decrease in risetime response for 0.35 volts input is due to M5 becoming cut off. Note that the fall time response initially decreases at higher input signal levels but then slows down as the output returns to its Q-point. This behavior is consistent with that of real neurons [4].

The circuit's behavior as an integrator is illustrated in Figure 4. The input signal consists of 5 equally-spaced 0.25 volt pulse with 10 nsec rise and fall times and a total width of 40 nsec. V_{GR} was set at 1.3 volts. We may note the rapid integration of the pulse inputs and the slow decay of the response tail at the cessation of the input. Also worthy of note is the fact that the tail's decay takes place over an interval of a few microseconds despite the absence of any explicitly-integrated capacitors in the circuit. This result demonstrates that passive integrated capacitor components are not necessary in pulse-mode artificial neurons since the effect they are intended to model – namely, the integration of voltage in the neural membrane – can be obtained from the transistors themselves.

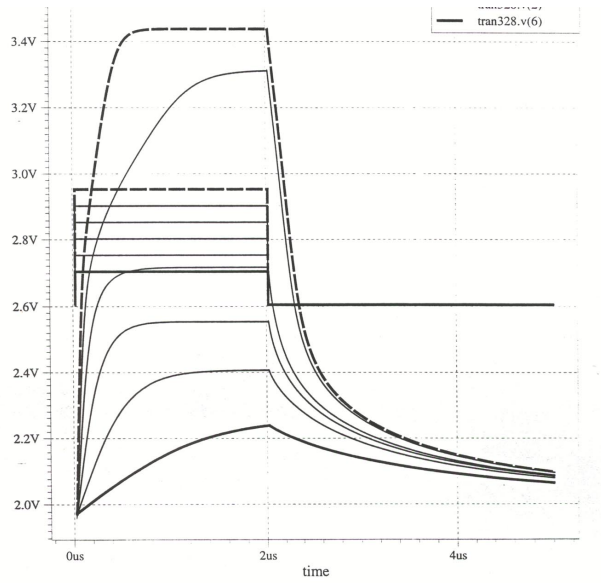

Fig. 3 Variation of pulse response as a function of input signal level (square pulse traces) for ac steps from 0.1 (bottom output trace) to 0.35 volts (top output trace) in 50 mV increments. V_{GR} = 1.3 volts.

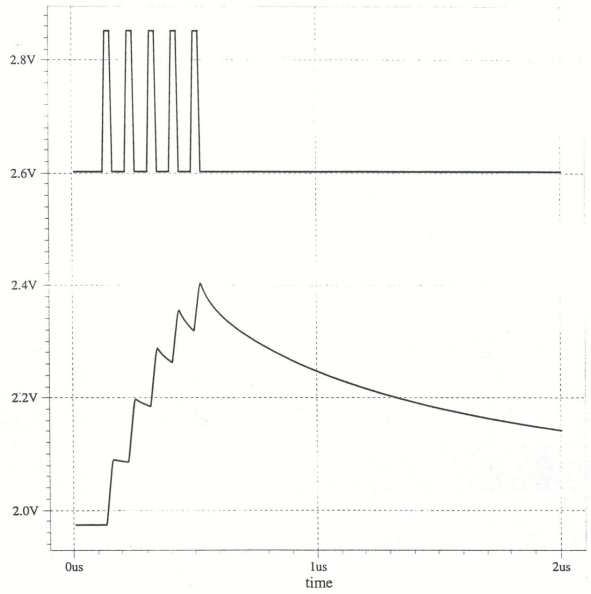

Fig. 4 Response of the circuit as an integrator. Note the rapid risetime response and slow falltime response, consistent with the behavior of real neurons.

Acknowledgement: This work was supported by the NSF-Idaho EPSCoR Program and by the National Science Foundation under award number EPS-0132626.

References

1. A.F. Murray, D.D. Corso, and L. Tarrasenko, "Pulse Stream VLSI Neural Networks Mixing Analog and Digital Techniques," *IEEE Trans. Neural Networks*, vol. 2, no. 2, 1991, pp. 193-204.
2. S.-C. Liu, "Silicon Photoreceptors with Controllable Adaptive Filtering Properties," in *Learning on Silicon*, Boston, MA: Kluwer Academic Publishers, 1999, pp. 67-78.
3. M. Banu and Y. Tsividis, "Floating Voltage-Controlled Resistors in CMOS Technology," *Electronic Lttrs*., vol. 18, no. 15, 1982, pp. 678-679
4. B. Hille, *Ion Channels of Excitable Membranes*, 3rd ed., Sunderland, MA: Sinauer Associates Inc., 2001, pp. 61-93.